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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,968	03/24/2004	David Thomas	03-2597	4466

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LSI Logic Corporation
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EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/807,968	THOMAS, DAVID	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
8/16/2006

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 6 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6 and 11 recite the limitations "wherein padding" and "said storage" in claims 6 and 11, line 1 respectively. There is insufficient antecedent basis for this limitation in the claim.

As per claim 6 and 11, it appears unclear as to what "padding" and which "storage" the applicant is referring to, as there appears to have no prior recitation of the claimed limitations "padding" and "storage" in the independent claims 1 and 7, which the dependent claims 6 and 11 are dependent on respectively. Examiner will assume "padding can only be added to received data to be buffered at the beginning of the transmission" for the current examination.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-6, 12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Jaquette et al. (US Patent 6,009,547).

3. As per claims 1 and 12, Jaquette teaches a method and a computer program product stored on a computer readable medium to be executed for protecting data as it passes through a buffering device (Fig. 1, ref. 10, 16) that connects protocols that use different block sizes or unblocked data (col. 4, ll. 8-50, wherein the data received from the host system is unblocked as padding may be utilized to form blocks of data), comprising:

receiving data on a first port (col. 3, ll. 1-6), wherein the first port is the interconnection between the memory system (Fig. 1, ref. 10) and the host system (Fig. 1, ref. 12) and data is received from the host system;

storing said data in a first memory (DRAM 16 of Fig. 1) in said buffering device such that said data is stored in a plurality of blocks, each block having a length of 2^n, where n is a positive number (col. 5, ll. 13-26), wherein data inputted is stored in the memory segment of the DRAM specifically for data blocks, having the block size of 2^7=128 bytes, wherein n=7;

calculating a first cyclical redundancy code for each of said plurality of blocks as each of said plurality of blocks is written (col. 4, ll. 24-27), wherein the first cyclical redundancy codes corresponds to the ECC check symbols calculated;

when a first block of said plurality of blocks is completed, storing a corresponding first cyclical redundancy code in a second memory on said buffering device (col. 5, ll. 13-26), wherein the first cyclical redundancy codes corresponds to the ECC check

symbols are stored in a different segment of the DRAM from where the data blocks are stored;

a second port (Fig. 1), wherein the second port is the interconnection between the memory system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14); and

when writing said data to the second port, computing a second cyclical redundancy code (e.g. four ECC bytes) for each of said blocks of said plurality of blocks and if said second cyclical redundancy code corresponding to a given block is equal to said first cyclical redundancy code corresponding to said given block, writing said given block to said second port (col. 9, ll. 22-48).

4. As per claim 4, Jaquette teaches the method comprising wherein one of said first and said second ports is connected to a protocol that does not use fixed block lengths (col. 4, ll. 42-50), wherein data received from said first port is connected to the protocol that does not use fixed block length as data received are padded to form the fixed block length.

5. As per claim 5, Jaquette teaches the method comprising wherein locations in said second memory are mapped to locations in said first memory (col. 5, ll. 26-37), wherein the mapping is implemented utilizing an offset from the data block partitions.

6. As per claim 6, Jaquette teaches the method comprising padding can only be added to received data to be buffered at the beginning of the transmission (col. 4, ll. 42-

50), wherein padding is added to the received data to form blocks of data of 32 bytes at the beginning of the transmission to the DRAM (i.e. before storing the received data into DRAM).

7. As per claim 14, Jaquette teaches the computer program product stored on a computer readable medium to be executed comprising wherein said computer program product is embodied on a protocol interface device (Fig. 1, ref. 10, 16) connected between a bus and a tape drive (e.g. magnetic tape) (col. 4, ll. 8-13), wherein the bus is the interconnection between the host system (Fig. 1, ref. 12) and the memory system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14) may be a magnetic tape.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaquette et al. (US Patent 6,009,547) in view of Hogan et al. (US Patent 6,765,739).

Jaquette teaches all the limitations of claims 1 and 12 as discussed above, wherein Jaquette further teaches the method comprising checking the data with ECC for error (col. 6, ll. 46-59).

Jaquette does not teach the method comprising wherein the data is received with a protection code that is checked and discarded.

Hogan teaches a system and a method comprising receiving an encoded data (Fig. 2, ref. 32) (i.e. protection code) and removing (i.e. discard by removing) the ECC from the received encoded data (Fig. 2, ref. 36).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hogan's receiving and removing ECC from received data into Jaquette's method. The resulting combination of the references teaches the method further comprising wherein the data received is encoded with ECC (i.e. protection code) and the checking and removing of the ECC.

Therefore, it would have been obvious to combine Hogan with Jaquette for the benefit of providing copy protection data to be written onto the data storage system such as a disk (Hogan, col. 3, ll. 27-45).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaquette et al. (US Patent 6,009,547) in view of "PCTechGuide".

Jaquette teaches all the limitations of claim 1 as discussed above, wherein Jaquette further teaches the method comprising wherein said buffering device is a DRAM device (Fig. 2, ref. 16) connected between a bus and a tape drive (data storage device 14 of Fig. 1) (col. 4, ll. 8-13), wherein the bus is the interconnection between the host system (Fig. 1, ref. 12) and the memory system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14) may be a magnetic tape.

Jaquette does not teach the method comprising wherein the DRAM device is a DDR device.

PCTechGuide teaches a system and a method comprising transferring data utilizing DDR DRAM (DDR DRAM Section, 2nd paragraph on page 3).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include PCTechGuide's DDR DRAM into Jaquette's memory system.

Therefore, it would have been obvious to combine PCTechGuide with Jaquette for the benefit of allowing data to be transferred faster as data can be transferred during both the rising edge and falling edge of the clock (DDR PCTechGuide, DDR DRAM Section, 2nd paragraph on page 3).

10. Claims 7-8 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jaquette et al. (US Patent 6,009,547) in view of Malakapalli et al. (US Patent 6,467,060).

11. As per claim 7, Jaquette teaches a device for buffering data between two protocols, at least one of which does not utilize blocks (col. 4, ll. 8-50, wherein one protocol conforms to a host system and the other protocol conforms to a data storage system and the protocol associated with the host system does not utilize blocks as data received from the host system may need to be padded to form blocks), said device comprising:

a first port connected to communicate using a first protocol of said two protocols (Fig. 1), wherein the first port is the interconnection between the memory system (Fig. 1, ref. 10) and the host system (Fig. 1, ref. 12), conforming to the protocol utilized by the host system;

a second port connected to communicate using a second protocol of said two protocols (Fig. 1), wherein the second port is the interconnection between the memory system (Fig. 1, ref. 10) and the data storage system (Fig. 1, ref. 14), conforming to the protocol utilized by the data storage system;

a cyclical redundancy code engine (CRC generator circuit 20 of Fig. 1) connected to be selectively connected to one of said first port and said second port (col. 4, ll. 24-27 and col. 10, ll. 9-23), as the cyclical redundancy code for each of the data inputted from each of the respective port is generated by the CRC generator circuit, therefore the CRC generator circuit is selectively coupled to the respective port, depending on which port is inputting data;

a first random access memory (Fig. 1, ref. 16) connected to said cyclical redundancy code engine (Fig. 1, ref. 20) and in which data passing between said first port and said second port is stored in a plurality of fixed size blocks (col. 4, ll. 24-27 and col. 5, ll. 13-26), wherein data inputted is stored in the memory segment of the DRAM specifically for data blocks, having the fix block size of 2^7=128 bytes;

a second random access memory (Fig. 1, ref. 16) connected to said cyclical redundancy code engine (Fig. 1, ref. 20) and in which said first cyclical redundancy codes corresponding to said fixed size blocks are stored (col. 4, ll. 24-27 and col. 5, ll.

13-26), wherein the first cyclical redundancy codes corresponds to the calculated ECC check symbols are stored in a different segment of the DRAM from where the data blocks are stored; and

when writing said fixed size blocks of data to the second port, computing a second cyclical redundancy code (e.g. four ECC bytes) for each of said blocks of said plurality of blocks and if said second cyclical redundancy code corresponding to a given block is equal to said first cyclical redundancy code corresponding to said given block, writing said given block to said second port, therefore the data passed through said device is protected by a cyclical redundancy code (col. 9, ll. 22-48).

Jaquette does not expressly teach the device comprising a comparator connected to compare the second cyclical redundancy code with the first cyclical redundancy code when said fixed size blocks were written.

Malakapalli teaches a system and a method comprising a comparator (Fig. 13, ref. 1370) to compare the first cyclical redundancy code to the second cyclical redundancy code (col. 16, ll. 33-37).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Malakapalli's comparator into Jaquette's memory system.

Therefore, it would have been obvious to combine Malakapalli with Jaquette for the benefit of increasing the integrity of data stored on mass-storage (Malakapalli, col. 3, ll. 35-41).

12. As per claim 8, Jaquette and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising wherein said cyclical redundancy codes are stored in said second random access memory in a mapped relationship to said fixed size blocks stored in said first random access memory (Jaquette, col. 5, ll. 26-37), wherein the mapped relationship is implemented utilizing an offset from the data block partitions.

13. As per claim 10, Jaquette and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising wherein locations in said second random access memory are mapped to locations in said first random access memory (Jaquette, col. 5, ll. 26-37), wherein the mapping is implemented utilizing an offset from the data block partitions.

14. As per claim 11, Jaquette and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising padding can only be added to received data to be buffered at the beginning of the transmission (Jaquette, col. 4, ll. 42-50), wherein padding is added to the received data to form blocks of data of 32 bytes at the beginning of the transmission to the DRAM (i.e. before storing the received data into DRAM).

15. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jaquette et al. (US Patent 6,009,547) and Malakapalli et al. (US Patent 6,467,060), and further in view of Hogan et al. (US Patent 6,765,739).

Jaquette and Malakapalli teach all the limitations of claim 7 as discussed above, where Jaquette further teaches the device comprising checking the data with ECC for error (col. 6, ll. 46-59).

Jaquette does not teach the device comprising a protection module connected to said first port for checking a protection code that is received and discarding said protection code.

Hogan teaches a system and a method comprising receiving an encoded data (Fig. 2, ref. 32) (i.e. protection code) and removing (i.e. discard by removing) the ECC from the received encoded data (Fig. 2, ref. 36).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Hogan's receiving and removing ECC from received data into Jaquette's device. The resulting combination of the references teaches the device further comprising wherein the data received is encoded with ECC (i.e. protection code) and the checking and removing of the ECC, therefore, it would be obvious to have the protection module for implementing the functions just described.

Therefore, it would have been obvious to combine Hogan with Jaquette for the benefit of providing copy protection data to be written onto the data storage system such as a disk (Hogan, col. 3, ll. 27-45).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
08/17/2006

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